GaAs/InGaAs HETEROSTRUCTURE FETs WITH 1.6W OUTPUT POWER AT 1GHz

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ABSTRACT

Data are presented on high power GaAs/InGaAs pseudomorphic heterostructure FETs with delta doped channels, which are applicable for the low voltage operating celluar phone power modules. Process yields of such AlGaAs-free device are significantly improved in epitaxy and ohmic metalization. With a 5V Class A bias condition, the packaged device with a 1.2μm x 12mm gate exhibits a power output of 1.6W and a power added efficiency of 44-percent at 1GHz operation. The smaller device with a 1.2μm x 2mm gate shows a 160 mW output and a 34-percent efficiency at 2GHz with a 3.3V bias. These results imply that the GaAs/InGaAs HFET can be a strong candidate for the low cost commercial source of many kinds of high power microwave devices operating at relatively low operating voltages.

INTRODUCTION

Recent progress in the wireless personal telephone systems working at 0.85 or 2.4GHz bands has promoted commercial R&D activities for the development of high efficiency RF power devices operating at a low voltage region below 5V[1]. The AlGaAs/(In,Ga)As heterostructure FET (HFET), exhibiting high power outputs and high efficiencies in the X-band application[2,3], could be a good candidate for the specific commercial application such as the power module of hand-held celluar phone systems. However, the AlGaAs/(In,Ga)As HFET structure has several generic problems originating from the difficulties in epitaxial growth of the AlGaAs barrier heterojuction and ohmic contact formation through the lightly doped AlGaAs layer. To be accepted in the commercial market, such problems should be solved.

In an effort to avoid such difficulties encountered in the AlGaAs heterostructures and to explore the commercial market acceptability of our GaAs devices, we have proposed and fabricated the AlGaAs-free GaAs/InGaAs HFET structure with a delta doped channel[4]. This paper describes our work on MBE grown GaAs/InGaAs HFETs, which exhibits a good power output and a relatively high efficiency. Practical advantages of this pseudomorphic structure are also addressed.

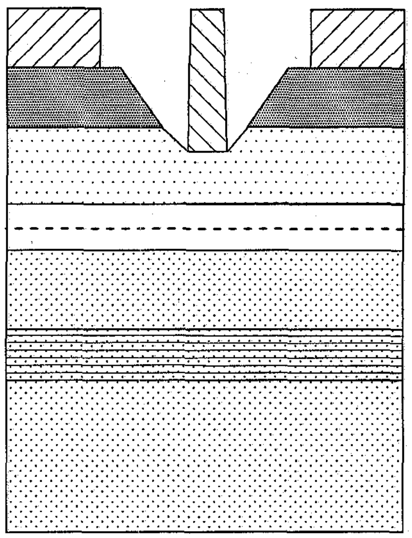

Figure 1. GaAs/InGaAs HFET with a delta doping channel in the InGaAs well.

DEVICE STRUCTURE AND FABRICATION

Our own MBE grown HFET structure is sketched in Figure 1. It consists of a n+$In_{0.2}Ga_{0.8}As$ contact layer, n-GaAs barrier, i-$In_{0.2}Ga_{0.8}As$ well, and a i-GaAs buffer layer with AlGaAs/GaAs superattice. The top n+$In_{0.2}Ga_{0.8}As$ layer is introduced in order to ensure the reliable ohmic contact and the superlattice buffer layer is inserted to suppress the substrate leakage current. The n-GaAs quantum barrier is lightly doped at mid $10^{16}cm^{-3}$ range to reduce the gate leakage current, yet to allow the good ohmic contact through the layer. To be noted, it is much easier in GaAs to make a reliable ohmic contact than in AlGaAs. The layer thickness is adjusted to yield a -2V cutoff.

The undoped $In_{0.2}Ga_{0.8}As$ includes a delta doped layer acting as a high carrier channel. Figure 2 shows the C-V concentration profile measured near across the delta doped layer. It proves that our MBE delta doping process provides the well confined quasi-two dimensional electron channel. The estimated two dimensional concentration is $1.4 \times 10^{12}/cm^2$. The electron mobility profile in the same figure is estimated with capacitances and transconductances measured in depth from our test FET. The profile reveals that the two dimensional channel mobility are relatively high above $3000 cm^2/V.sec$. These two profiles confirm that, in spite of the low band offset compared with the common AlGaAs/InGaAs junction, the carrier confinement of this structure is still good and the channel mobility is also high enough for common microwave applications.

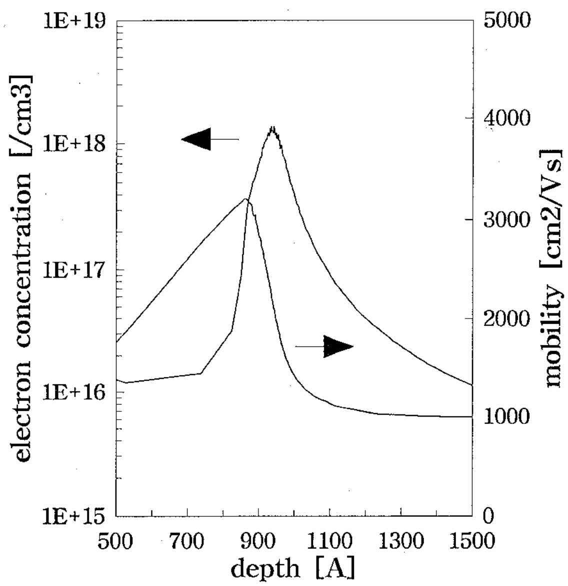

Figure 2. Profiles of quasi-two-dimensional electron concentration and mobility of MBE grown GaAs/InGaAs HFET structure.

The HFETs are fabricated with 3″ MBE wafers using the common 1.2μm FET processing techniques. Three different sized chips, with the total gate widths of 150μm, 2 and 12mm, are processed with one mask set. The 100μm gate chip is only for the DC test. The other two are completely processed for the RF power measurements. The Figure 3 illustrates the whole view of a 12mm gate HFET chip after wire bonding. The dimension of this chip is 0.8mm x 0.25mm. The gate has 80 unit fingers with a dimension of 1.2μm x 150μm. Among critical fabrication procedures are the elongate multiple gate recess and many air-bridge metal cross-overs. Figure 4 shows the magnified view of the well fabricated multi-fingered gates and air-bridge metal cross-overs after completing the device process.

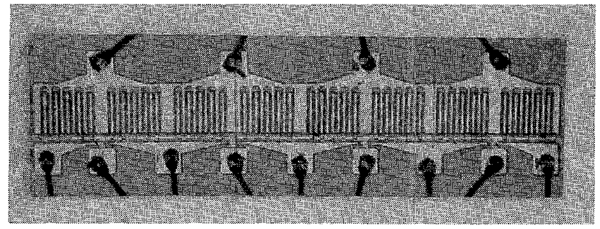

Figure 3. The whole view of GaAs/InGaAs HFET with 80 unit gate fingers. Dimension of the unit finger is 1.2μm x 12mm.

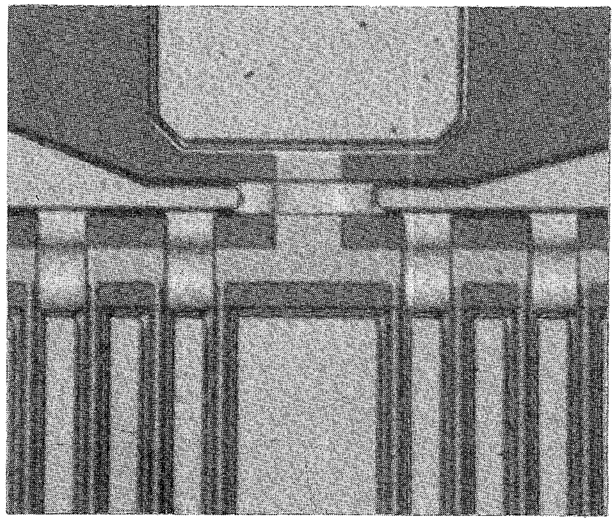

Figure 4. Air-bridge cross-over

In our chip fabrication process, the AlGaAs-free structure turns out to be more reliable and more consistent than the usual AlGaAs/InGaAs structure. We may attribute it to the similar optimum growth parameters of GaAs and InGaAs and also to the relatively easy ohmic contact process in GaAs. Also the quality control of the GaAs/InGaAs junction is likely to be more consistent than AlGaAs/InGaAs junction's. To be noted that the AlGaAs growth is somewhat inconsistent due to the naturally strong oxidation tendancy of aluminum.

DC AND RF CHARACTERISTICS

We measured the I-V characteristics of the test device to understand the DC characteristics of our GaAs/InGaAs HFET structure. Figure 5 shows the transconductance and drain current as a function of gate voltage with the drain voltage at 3V. The transconductance is almost constant, as expected from the device with delta doped channel, near the value of 110mS/mm at the wide range of gate voltage. The drain current is 140mA/mm at the zero gate voltage and the cutoff voltage is -2.0V.

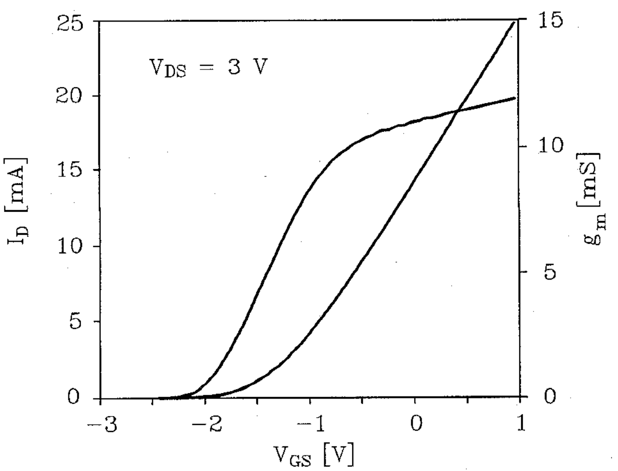

Figure 5. Transconductance and drain current of 100μm gate test HFET as a function of gate voltage,

For the real size device measurements, we have developed the thermally stable bonding process. Since our 12mm gate HFET chip is relatively large it should be more heat-resistive. A production type auto-bonding machine is used for the die attach, while a manual bonder is used for wire bonding. A few hundreds of HFETs were packaged in the commercially available common package units. Figure 6 shows a packaged 12mm gate device. All real device measurements of DC and RF characteristics have done with packaged devices in this way.

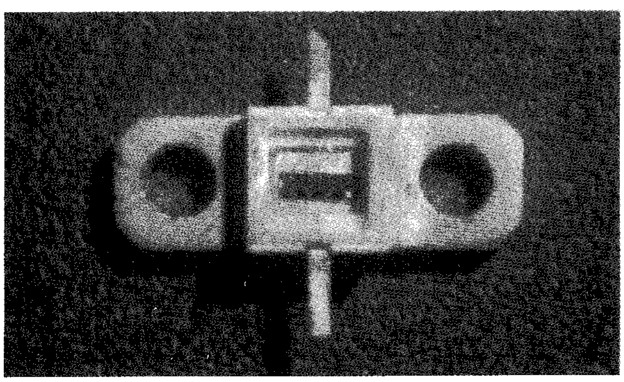

Figure 6. Packaged GaAs/InGaAs HFET

The typical I-V characteristics of the device shown in Figure 6 are shown in Figure 7. The device is well saturated with a drain current near 1.8A at zero gate voltage, and shows good pinch off at 2.0V. The knee voltage is near 1.7V at 1.6A(or 133mA/mm) drain voltage. The transconductance is basically identical to the one measured from the test device as shown in Figure 5. The usual breakdown voltage is above 16V which is high enough to derive the high power to this device. At a Class A type bias at 5V-1.1A, the expected maximum power output from this device is 2.0W. The cutoff frquency and maximum frequency estimated from the S-parameter measurements (not shown here) are 2 and 6GHz, respectively. From the 2mm gate HFET (not shown here) those values are estimated as 11.8 and 13.1GHz, respectively.

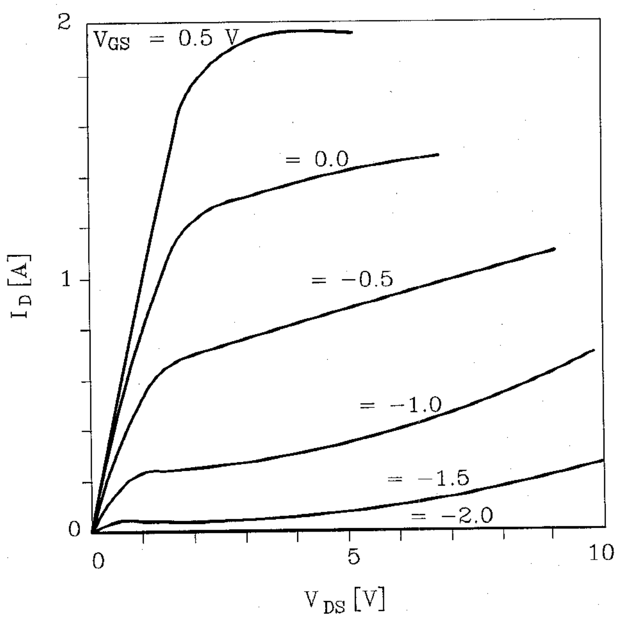

Figure 7. I-V characteristics of HFET (12mm gate).

Figure 8 shows the RF characteristics of the typical 12mm gate HFET measured at 1GHz region with a Class A bias condition of 5V and 760mA. The maximum output power of this HFET is 32.1 dBm (or 1.6watts) at 1dB saturation point with 18.7dBm (or 74.5mW) input power. The power added efficiency measured at the same Class A bias condition is 44 percents. The power density per gate width is 0.13W/mm. The 2mm gate HFETs were tested at 2GHz with 3.3V bias (also tuned for the Class A operation). The measured output power and efficiency of this HFET were 160mW and 34 percents, respectively. The efficiency figures may be improved by pushing the drain current above

200mA/mm and lowering the bias voltage. However, if we derive the device such a high current level we may encounter the thermal unstability problem.

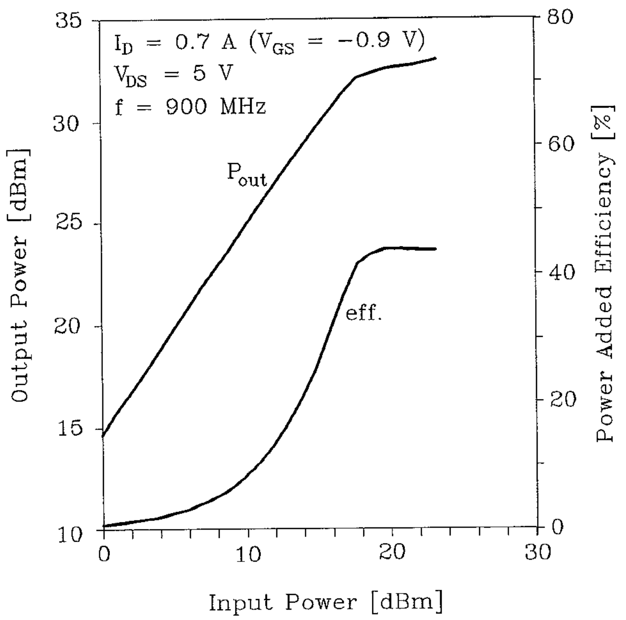

Figure 8. Output power and power added efficiency of GaAs/InGaAs HEFT(12mm gate)

CONCLUSION

The GaAs/InGaAs structure has not been much explored for the microwave device applications because its energy offset is smaller than AlGaAs/InGaAs junction's. However, the AlGaAs-free structure has certain advantages in epitaxy and ohmic process as well as in the natural junction quality. Such advantages can be addressed more clearly with an aid of delta doping technique, which provides a high carrier density channel without losing much mobility. Our HFET results confirm that the fabrication processes of GaAs/InGaAs HFET are more reliable and the quality control is more consistent than the AlGaAs/GaAs HFET's. High yielding processes are expected. Our 1GHz power data, 1.6W at 4.7V, implicates that such devices can be used for the commercial microwave power device applications. The 2GHz power data, 160mW at 3.3V, tells that extended works even to the high frequency band is necessary. In the short term strategy, the cascade amplifier consisting of two HFETs (2 mm and 12 mm) can be proposed for the celluar phone power module. Further applications for the low noise HEMTs, high power HBTs, and digital devices may be expected as well, in near future.

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REFERENCES

(1) T. Sawari, S. Murai and Y. Harada, "High efficiency GaAs power MESFETs and MMICs at very low drain bias.," Prceedings of 1993 Microwave Workshop and Exhibition, pp.365-368, Sept. 1993, Tokyo.

(2) P. Saunier, W. S. Kopp, H. K. Tserng, Y. C. Kao and D. D. Heston, "A Heterostructure FET with 75.8% Power Added Efficiency At 10GHz," 1992 IEEE MTT-S Digest, pp. 635-638.

(3) P. Smith,"PHEMT Power Appliers," Workshop on Microwave HBTs and HEMTs, IEEE-S Symp. 1993.

(4) E. F. Schubert, A. Fischer, and K. Ploog, "The delta-doped FET," IEEE Tran. Electron Dev. vol. ED-33, 1986.